## AMENDMENTS TO THE CLAIMS

**This listing of claims will replace all prior versions and listings of claims in the application:**

## LISTING OF CLAIMS:

1. (canceled).

2. (canceled).

3. (canceled).

4. (canceled).

5. (canceled).

6. (canceled).

7. (canceled).

8. (canceled).

9. (previously presented): A circuit board comprising a substrate and built thereon, a circuit comprised of a copper film,

wherein said copper film comprises an electroplated layer and has properties that (a) its crystallinity is such that the X-ray diffraction half-width of the (331) plane of copper is less than 0.3 deg. and (b) the variation in thickness ((maximum thickness-minimum thickness)/average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4.

10. (original): The circuit board according to Claim 9 wherein said copper film has an elongation of not less than 7%.

11. (previously presented): A printed circuit board comprising a substrate and, built thereon, a circuit comprised of a copper film,

wherein said copper film comprises an electroplated layer and has properties that (a) its crystallinity is such that the X-ray diffraction half-width of the (331) plane of copper is less than 0.3 deg. and (b) the variation in thickness ((maximum thickness-minimum thickness)/average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4.

12. (previously presented): A printed circuit board comprising a substrate formed with a conductor circuit, an interlayer resin insulating layer thereon and a conductor circuit comprised of a copper film on said interlayer resin insulating layer and having via holes by which said conductor circuits are interconnected,

wherein said copper film comprises an electroplated layer and has properties that (a) its crystallinity is such that the X-ray diffraction half-width of the (331) plane of copper is less than 0.3 deg. and (b) the variation in thickness ((maximum thickness-minimum thickness)/average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4.

13. (previously presented): The printed circuit board according to Claim 11 wherein said copper film has an elongation of not less than 7%.

14. (canceled).

15. (canceled).

16. (canceled).

17. (canceled).

18. (canceled).

19. (canceled).

20. (canceled).

21. (canceled).

22. (currently amended): A printed circuit board comprising a resin insulating substrate board formed with a roughened surface and, thereon, a conductor circuit comprising ~~at least~~ an electroless plated film and an electroplated film, wherein said electroless plated film is formed on a surface of said roughened surface and has a stress of 0 to +10 $kg/mm^2$.

23. (currently amended): A printed circuit board comprising a resin insulating substrate board formed with a roughened surface and, built thereon by semi-additive process, a conductor circuit comprising ~~at least~~ an electroless plated film and an electroplated film,

wherein said roughened surface comprises convex areas and concave areas, and said electroless plated film is complementary to a surface of said roughened surface with said electroless plated film in convex areas of said roughened surface being relatively greater in thickness than said electroless plated film in concave areas of said roughened surface.

24. (currently amended): A printed circuit board comprising a substrate board formed with a lower-layer conductor circuit and, built thereon by a build-up process, an upper-layer conductor circuit through the intermediary of an interlayer resin insulating layer, with said upper-layer conductor circuit and said lower-layer conductor circuit being interconnected by via holes,

wherein said lower-layer conductor circuit has a roughened surface, said upper-layer conductor circuit comprises ~~at least~~ an electroless plated film and an electroplated film, said interlayer resin insulating layer is provided with a roughened surface, with said electroless plated film being complementary to said roughened surface, ~~and~~

said interlayer resin insulating layer and said via holes are provided with the same electroless plated film, with said electroless plated film formed on the bottoms of said via holes having a thickness equal to 50 to 100% of the thickness of said electroless plated film on said interlayer resin insulating layer, and

said lower-layer conductor circuit and said electroless plated film formed on the bottom of said via hole are connected through said roughened surface of said lower-layer conductor circuit.

25. (currently amended): ~~A~~ The printed circuit board ~~comprising a resin insulating substrate board and thereon a conductor circuit comprising at least an electroless plated film~~ according to Claim 22,

wherein said electroless plated film is a copper film, and comprises at least one metal species selected from the group consisting of nickel, iron and cobalt.

26. (original): The printed circuit board according to Claim 25 wherein the proportion of said at least one metal species selected from the group consisting of nickel, iron and cobalt is 0.1 to 0.5 weight %.

27. (canceled).

28. (canceled).

29. (canceled).

30. (canceled).

31. (canceled).

32. (currently amended): A multilayer printed circuit board comprising a core board having on both sides ~~a~~ conductor ~~circuit~~ circuits and, over each of said conductor ~~circuit~~ circuits, buildup wiring layers comprising alternating an interlayer resin insulating layer and a conductor layer thereon, wherein the conductor layers are interconnected by via holes,

wherein said core board comprises a copper-clad laminate, each of said conductor circuit comprises a copper foil of said copper-clad laminate and a plated metal layer,

the thickness of each of said conductor circuit is not greater by more than 10 $\mu$m than the thickness of said conductor layer on said interlayer resin insulating layer~~, and~~

~~the thickness of said conductor circuit is substantially the same as the thickness of said conductor layer on said interlayer resin insulating layer~~.

33. (canceled).

34. (canceled).

35. (canceled).

36. (canceled).

37. (currently amended): A multilayer printed circuit board comprising a core board ~~and on both sides thereof~~ having on both sides conductor circuits and, over each of said conductor circuits, a buildup wiring ~~layers~~ layer comprising alternating an interlayer resin

insulating layer and a conductor layer thereon, wherein said conductor layers are interconnected by via holes,

wherein said core board is a copper-clad laminate, and is provided with plated-through holes, said conductor circuits comprise a copper foil of said copper-clad laminate and a plated film, and said via holes are formed immediately over said plated-through holes in the manner of plugging the through holes in said plated-through holes and are interconnected with said plated-through holes.

38. (original): The multilayer printed circuit board according to Claim 37 wherein the through holes in said plated-through holes have a diameter of not more than 200 $\mu$m.

39. (canceled).

40. (previously presented): A multilayer printed circuit board comprising a core board and on both sides thereof, buildup wiring layers comprising alternating an interlayer resin insulating layer and a conductor layer thereon, wherein the conductor layers are interconnected by via holes,

wherein said core board is provided with plated-through holes, and lower-layer via holes are disposed immediately over said plated-through holes, said plated-through holes being interconnected with said lower-layer via holes, and upper-layer via holes are disposed immediately over said lower-layer via holes, said upper-layer via holes being interconnected with said lower-layer via holes.

41. (previously presented): A multilayer printed circuit board comprising a core board and, on both sides thereof, buildup wiring layers comprising alternating an interlayer resin

insulating layer and a conductor layer thereon, wherein the conductor layers are interconnected by via holes,

wherein said core board is provided with plated-through holes, and said plated-through holes are filled with a filler, with the surfaces of said filler which are exposed from said plated-through holes being covered with said conductor layer provided with lower-layer via holes, and upper-layer via holes are disposed immediately over said lower-layer via holes, said lower-layer via holes being interconnected with said upper-layer via holes.

42. (previously presented): A multilayer printed circuit board comprising a core board and, on both sides thereof, buildup wiring layers comprising alternating an interlayer resin insulating layer and a conductor layer thereon, wherein the conductor layers are interconnected by via holes,

wherein said core board is provided with plated-through holes, and lower-layer via holes are disposed to plug through holes of said plated-through holes, said plated-through holes being interconnected with said lower-layer via holes, and upper-layer via holes are disposed immediately over said lower-layer via holes, said upper-layer via holes being interconnected with said lower-layer via holes.

43. (original): The multilayer printed circuit board according to any of Claims 40 to 42 which comprises bumps formed immediately above said plated-through holes.

44. (currently amended): The multilayer printed circuit board according to any of Claims 40 to ~~43~~42, wherein said lower-layer via holes are filled with metal.

45. (original): The multilayer printed circuit board according to any of Claims 40 to 42 wherein valleys of said lower-layer via holes are filled with a conductive paste.

46. (original): The multilayer printed circuit board according to any of Claims 40 to 42 wherein valleys of said lower-layer via holes are filled with a resin.

47. (canceled).

48. (previously presented): The circuit board according to Claim 9, wherein said copper film is formed by constant-voltage pulse plating technique.

49. (previously presented): The printed circuit board according to Claim 11, wherein said copper film is formed by constant-voltage pulse plating technique.

50. (previously presented): The printed circuit board according to Claim 12, wherein said copper film has an elongation of not less than 7%.

51. (previously presented): The printed circuit board according to Claim 12, wherein said copper film is formed by constant-voltage pulse plating technique.

52. (previously presented): The printed circuit board according to Claim 22, wherein said electroless plated film is formed from an electroless plating solution comprising tartaric acid or a salt thereof.

53. (previously presented): The printed circuit board according to Claim 23, wherein said roughened surface comprises a primary anchor and a secondary anchor, said primary anchor having concave and convex parts and said secondary anchor being formed on the convex areas of said roughened surface.

54. (previously presented): The printed circuit board according to Claim 24, wherein said electroless plated film is formed from an electroless plating solution comprising tartaric acid or a salt thereof.

55. (previously presented): The printed circuit board according to Claim 24, wherein said via holes have a diameter of 80 $\mu$m or less.

56. (previously presented): The printed circuit board according to Claim 25, wherein said electroless plated film comprises an alloy of copper and at least one metal species selected from the group consisting of nickel, iron and cobalt.

57. (previously presented): The multilayer printed circuit board according to Claim 32, wherein said conductor circuit on said core board is a conductor layer interconnected with a plated-through hole.